A 240 W Power Heterojunction FET with High Efficiency for W-CDMA Base Stations

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Abstract

An L/S-band highly efficient 240 W GaAs FET amplifier has been developed. The amplifier employed newly developed pseudomorphic heterojunction FETs (HJFETs) exhibiting large drain current and high gm characteristics. In addition, we employed the second harmonic tuning for the input and output matching circuit to obtain the high efficiency characteristics. The developed push-pull amplifier demonstrated 53.8-dBm (240 W) output power with 50 % power added-efficiency and 12-dB linear gain at 2.12 GHz. It also showed low adjacent channel leakage power ratio (ACPR) of less than -35 dBc with a power-added efficiency of 28 % at an output power of 45 dBm. The developed amplifier is suitable for digital cellular base station applications.

Introduction

High output power transistors of over 200 W are strongly required to realize the size-reduction of a base station amplifier. Especially, the final stage transistors in the solid-state power amplifiers (SSPAs) used for W-CDMA base stations are demanded to provide both high efficiency and low distortion characteristics with high saturation output power. In order to improve the power-added efficiency, Class-B operation is commonly employed, although it sacrifices the distortion characteristics and linear gain. In a power amplifier, the third order intermodulation (IM3) is dominated by the third order transconductance coefficient ($gm3 = d^3Id/dVg^3$) derived from a Volterra series expansion for the drain current. We found that FET with a steep gm-profile exhibits better symmetry and smaller value for gm3 at low current bias point [1].

In this work, to realize low distortion and high gain characteristics at low current operation, we employed a double-doped pseudomorphic heterojunction FET (HJFET) which gives both high gm and small gm3 values. Moreover, we employed the second harmonic tuning for the input matching circuit as well as output matching circuit to obtain the high efficiency characteristic.

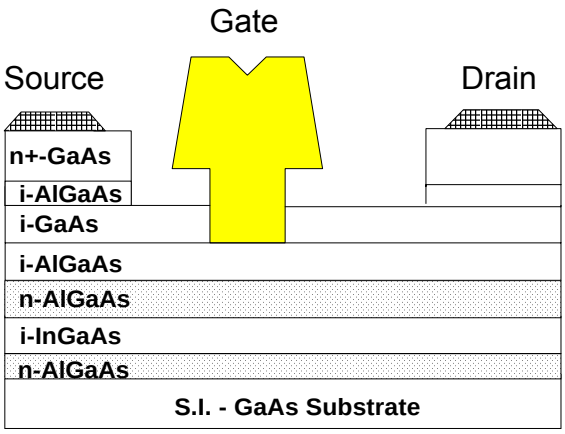

Fig. 1 Cross sectional view of the developed pseudomorphic HJFET.

Device structure and Chip Design

A schematic cross-section of the fabricated double-doped pseudomorphic HJFET is shown in Fig. 1. An offset-gate structure was adopted to obtain a high gate-drain breakdown voltage (BVgd) of more than 30V, which is required to enable high voltage (12 V) amplifier operation. We fabricated HJFETs using a selective dry etching process for the precise control of the threshold voltage (Vth) and Au/WSi gate metallization technology. In order to obtain the steeper gm-profile, we experimentally optimized Vth, epitaxial layer structure and recess structures of the device. Since the linear gain and the third-order distortion depend on gm and gm3/gm, respectively, our HJFETs enable low distortion and high gain characteristics at low current operation.

Figure 2 shows the photograph of the FET chip used in a push-pull amplifier. The total gate width is 150 mm and chip size is 1.3×4 mm^2. The gate-pitch and the finger-width were 17 µm and 680 µm, respectively, optimized for trade-off relationship between the thermal resistance and the RF linear gain of the device. The GaAs substrate

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was thinned to 40 µm and a gold plated-heat-sink with a thickness of 15 µm was formed on the backside of the substrate in order to reduce the thermal resistance. Air-bridges and via-holes were used to reduce the parasitic capacitance and inductance. The typical maximum drain current (Imax), gm, Vth, and BVgd are 400 mA/mm, 280 mS/mm, -0.5 V and 31 V, respectively. The breakdown voltage is sufficiently high to operate under the drain bias voltage of 12 V.

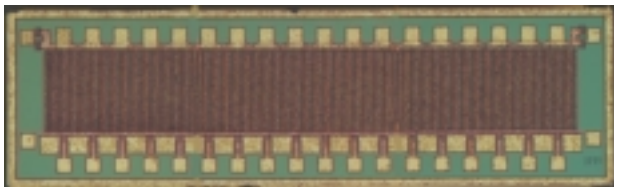

Fig. 2 Photograph of HJFET chip

Circuit Design

We simulated the influence of the second harmonic source impedance as well as the second harmonic load impedance on the power-added efficiency (PAE), using a large signal model (Agilent EEHEMT1 model) extracted for our device. Using a unit cell model, we performed the second harmonic (2f0 = 4.2 GHz) source-pull and load-pull simulation while keeping the same fundamental (f0 = 2.1 GHz) load condition for maximizing efficiency. Figure 3 shows the PAE contours at the 2dB-gain compression operation point on the second harmonic load-pull simulation. The second-harmonic load impedance dependence on PAE indicated that the second harmonic impedance for high efficiency should be open condition rather than short condition. This result is opposite to the Class-F terminal condition [2] on the second-harmonic load impedance. Figure 4 shows the PAE contours at 2dB-gain compression operation point on the second harmonic source-pull simulation. A high efficiency was obtained at around short condition for the source impedance at the second harmonic. In addition to the load second harmonic impedance, the source second harmonic impedance plays an important roll for high efficiency operation.

Using the newly developed pseudomorphic HJFETs, we designed the L/S-band push-pull amplifier. The overall developed amplifier circuit is shown in Fig. 5. Two pairs of GaAs HJFET chips (i.e. total Wg = 4 × 150 mm) were mounted on a single package with pre-matching circuits. The output-power was combined in push-pull configuration with external balun circuits. The package size is 17 × 34 mm^2. Figure 6 shows the top view of the internally matched device. The internal input matching circuit consists of a two-stage LC low pass filter network in order to realize short condition for second harmonic source impedance. The internal output matching circuit consists of transmission lines and one-stage LC low pass filter networks in order to realize open condition for the second harmonic load impedance.

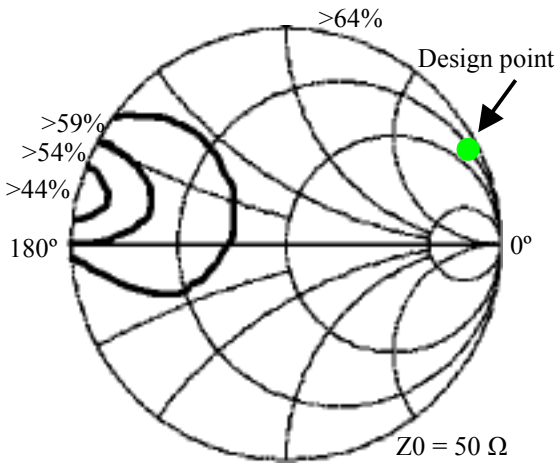

Fig. 3 PAE contours at the 2dB-gain compression operation point on the second harmonic load-pull simulation.

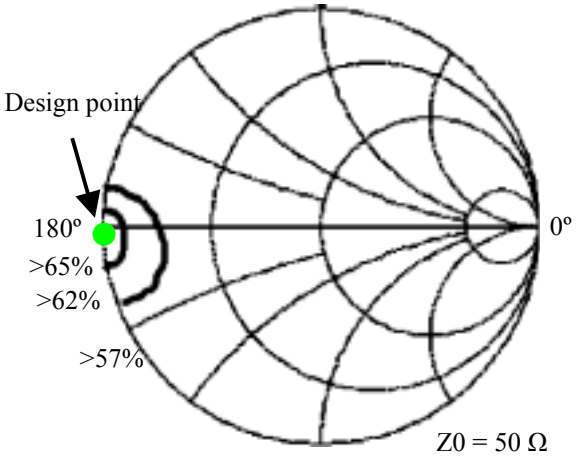

Fig. 4 PAE contours at the 2dB-gain compression operation point on the second harmonic source-pull simulation.

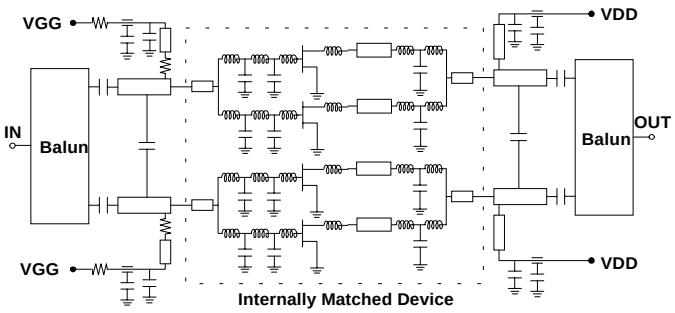

Fig. 5 Overall push-pull amplifier circuit.

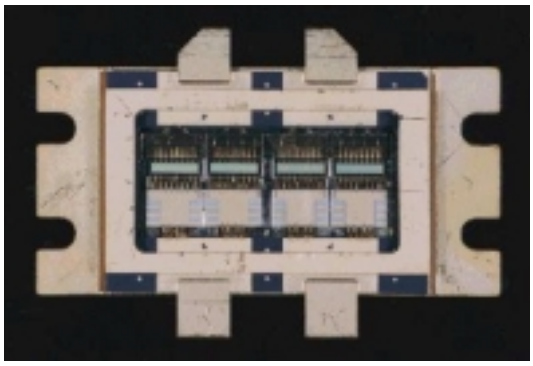

Fig. 6 Photograph of the developed internally matched device.

Amplifier Performance

Measured output power and power-added efficiency versus input power are shown in Fig. 7. When the developed amplifier was tuned for the maximum output power, it exhibited a saturation output power (Psat) of 53.8 dBm (240 W) with a linear gain of 12 dB and a PAE of 50% at 2.12 GHz at a drain-source voltage (Vds) of 12 V with a quiescent drain-source current (Idsq) of 1.5 A, which is 0.5 % of the Imax. When the device was tuned for the maximum efficiency, it delivered a Psat of 53.2 dBm (209 W) with a linear gain of 13.2 dB and a PAE of 53%. Figure 8 shows the adjacent channel leakage power ratio (ACPR) characteristics and PAE measured with a W-CDMA modulation signal. Low ACPR of -34 dBc with a 26 % PAE was obtained at an output power of 46 dBm at tuning for the maximum output power. By tuning for the maximum efficiency, 28% PAE with a -35 dBc ACPR was achieved at an output power of 45 dBm. IM3 versus total output power with two W-CDMA signals of the 15 MHz-carrier spacing (2.1125 GHz, 2.1275 GHz) is shown in Fig. 9. The amplifier exhibited low IM3 characteristics of less than -30 dBc with a 28 % PAE at the total output-power of 45 dBm. Figure 10 illustrates the spectrum at an output-power of 45 dBm when driven with two W-CDMA signals of the 15MHz-carrier spacing. The amplifier exhibited low intermodulation performance of less than -30 dBc on both the upper and lower side of the carriers. Excellent power performance at the 8-dB back-off power level from Psat was required for W-CDMA base station system applications. Figure 11 compares the 8-dB back off power performance for reported S-Band high-power FETs [3, 4]. We achieved the highest efficiency at the operation power point of 8-dB back off from Psat. It is notable that this high efficiency with low distortion characteristics was obtained at low Idsq.

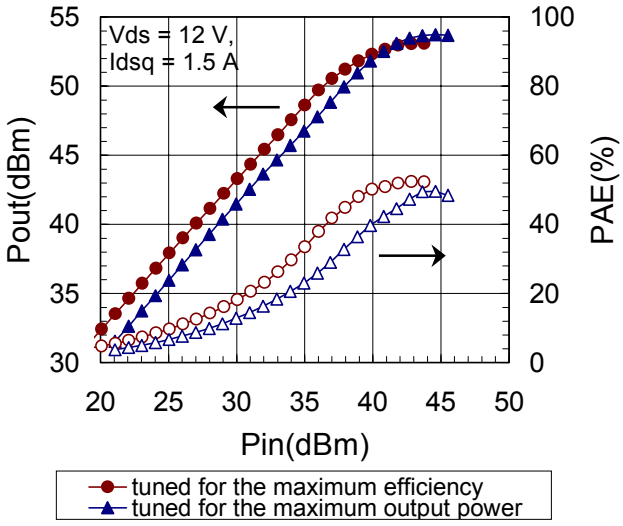

Fig. 7 Output power and power-added efficiency versus input power of developed push-pull amplifier at 2.12 GHz.

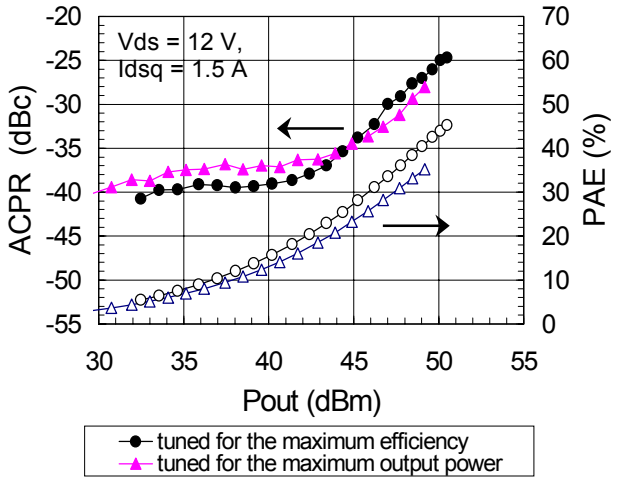

Fig. 8 ACPR and PAE with a W-CDMA modulation signal at 2.12 GHz.

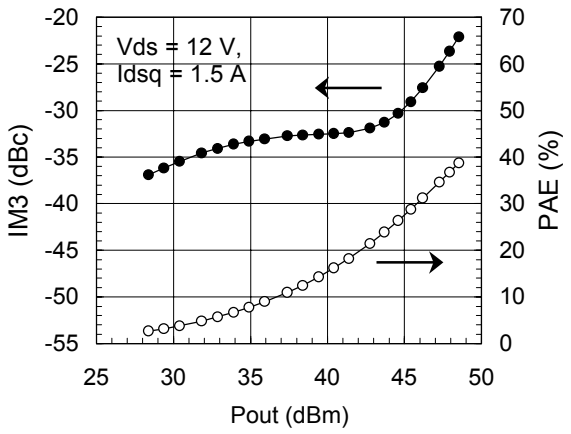

Fig. 9 IM3 versus total output power with two W-CDMA signals (2.1125 GHz, 2.1275 GHz).

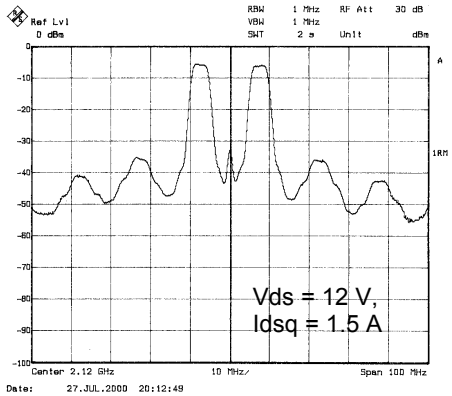

Fig. 10 Spectrum at an output-power of 45 dBm when driven with two W-CDMA signals (2.1125 GHz, 2.1275 GHz).

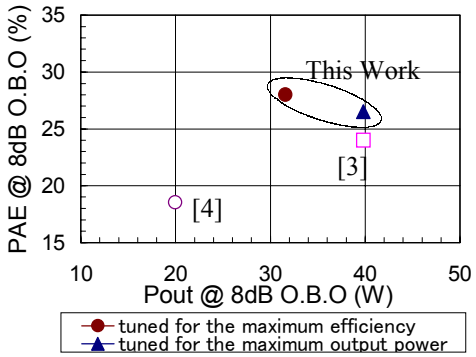

Fig. 11 PAE at the 8-dB back-off power level from Psat under W-CDMA condition of the developed power amplifier in comparison with reported S-Band high-power FETs.

Conclusions

An L/S-band highly efficient 240 W GaAs FET amplifier has been developed. At 2.12 GHz, an output power of 240 W has been obtained with 50 % power added-efficiency and 12 dB linear gain. Under W-CDMA signal test condition, the amplifier exhibited low ACPR performance of less than –35 dBc with a power-added efficiency of 28 % at an output-power of 45 dBm. The developed GaAs HJFETs are promising for the 3rd generation digital cellular base station applications.

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